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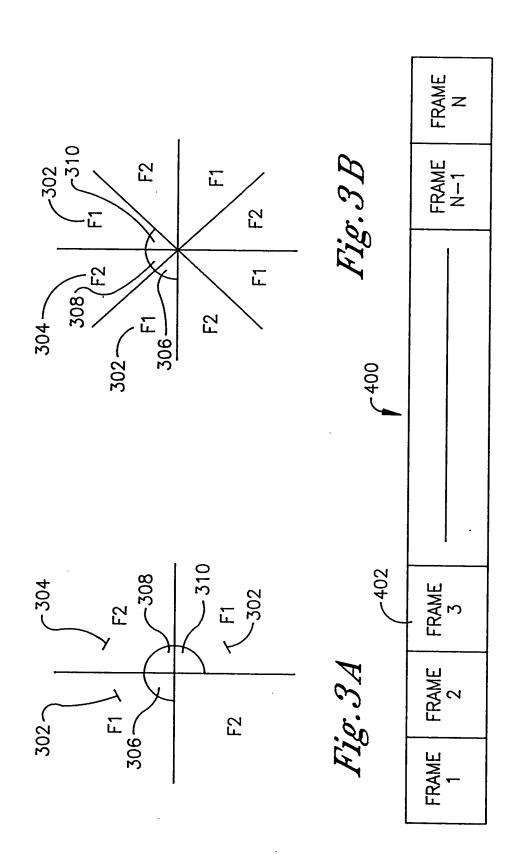
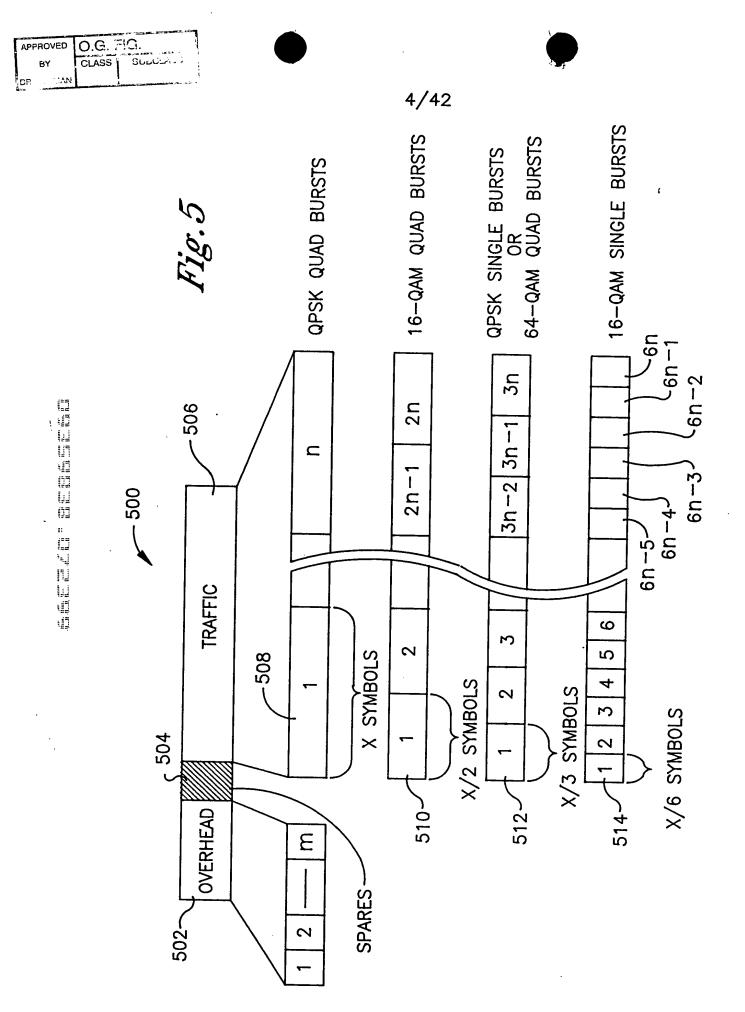
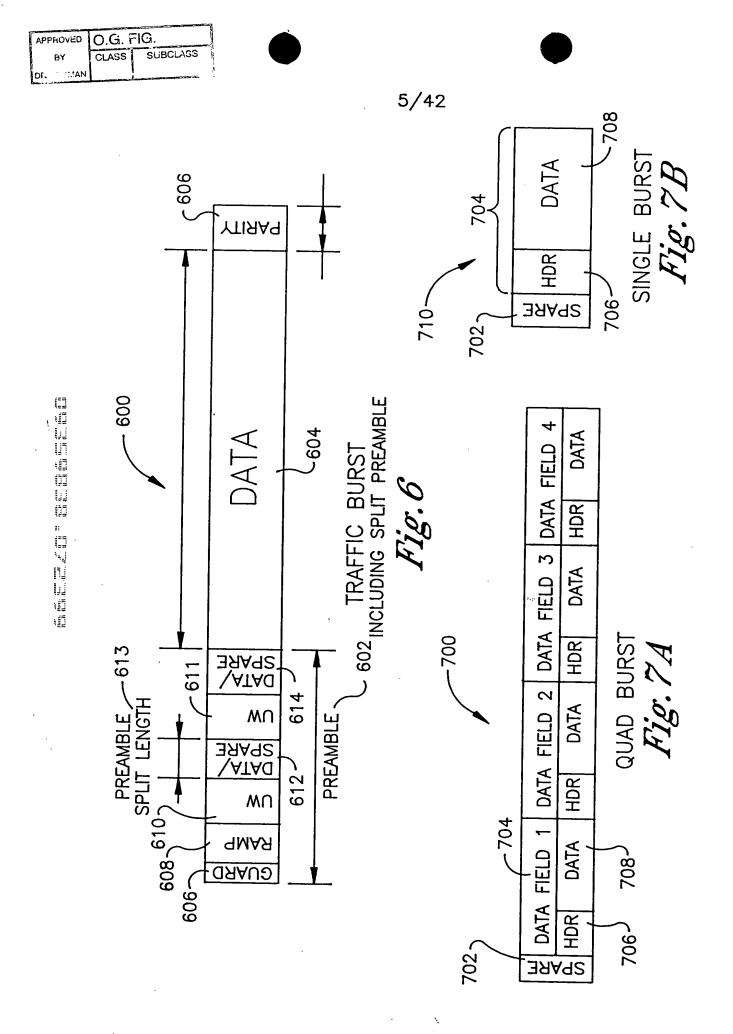


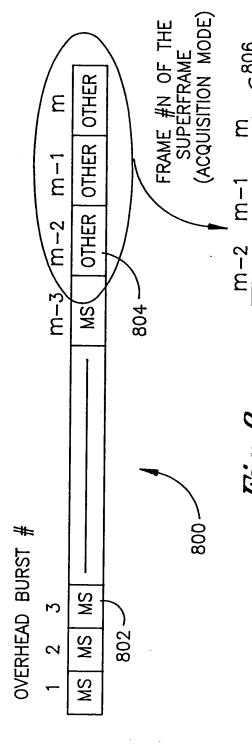
Fig. 4

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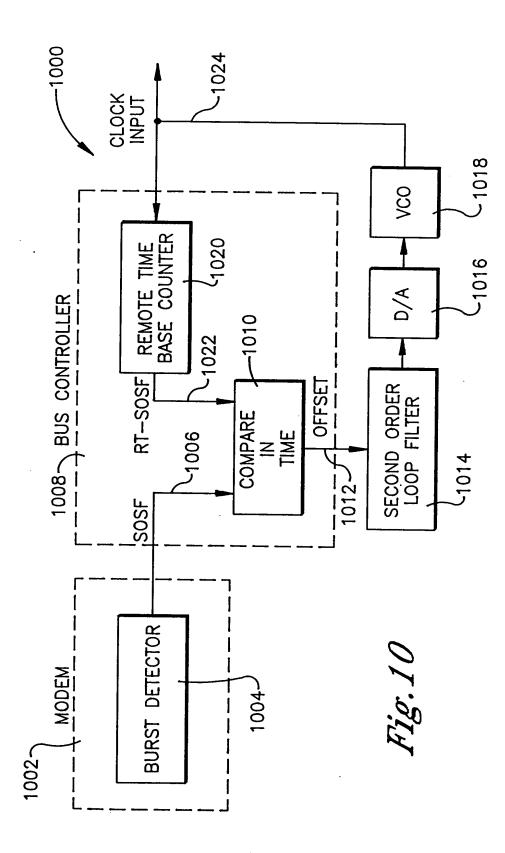


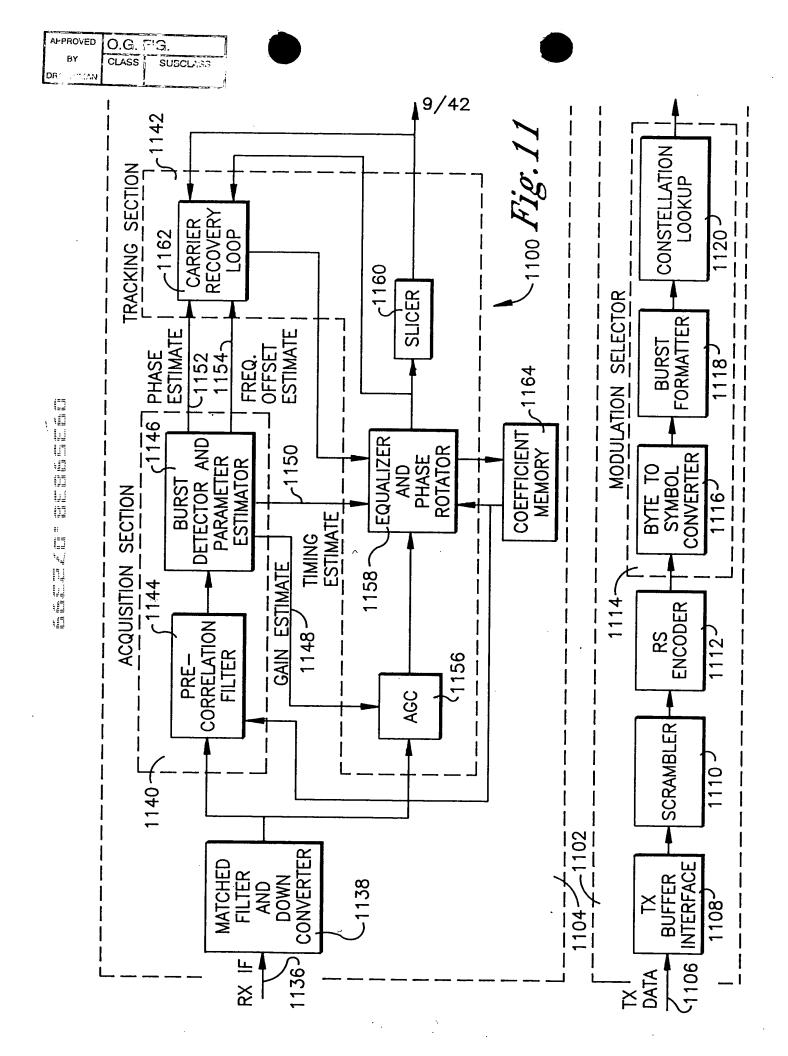


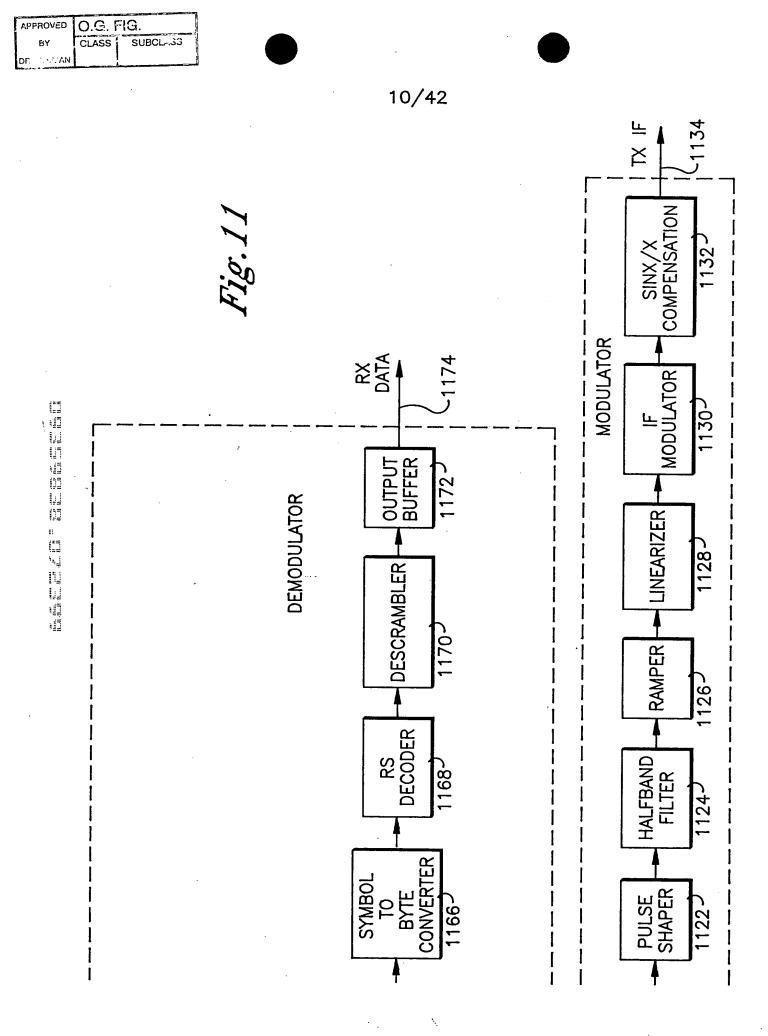
ACQUISITION SLOT

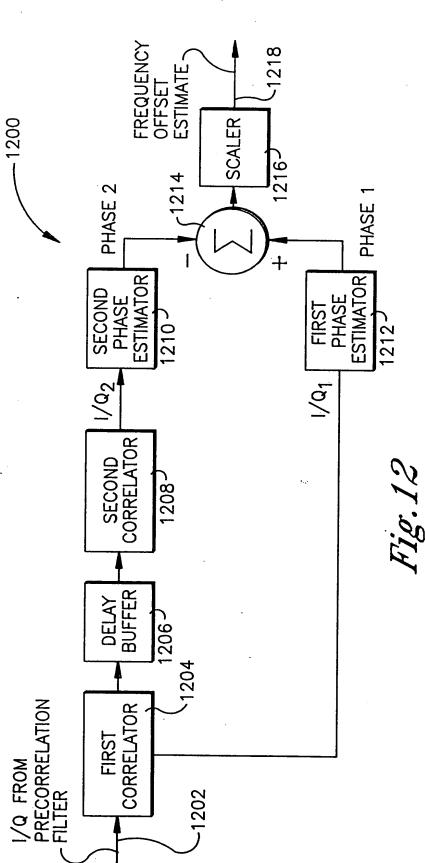


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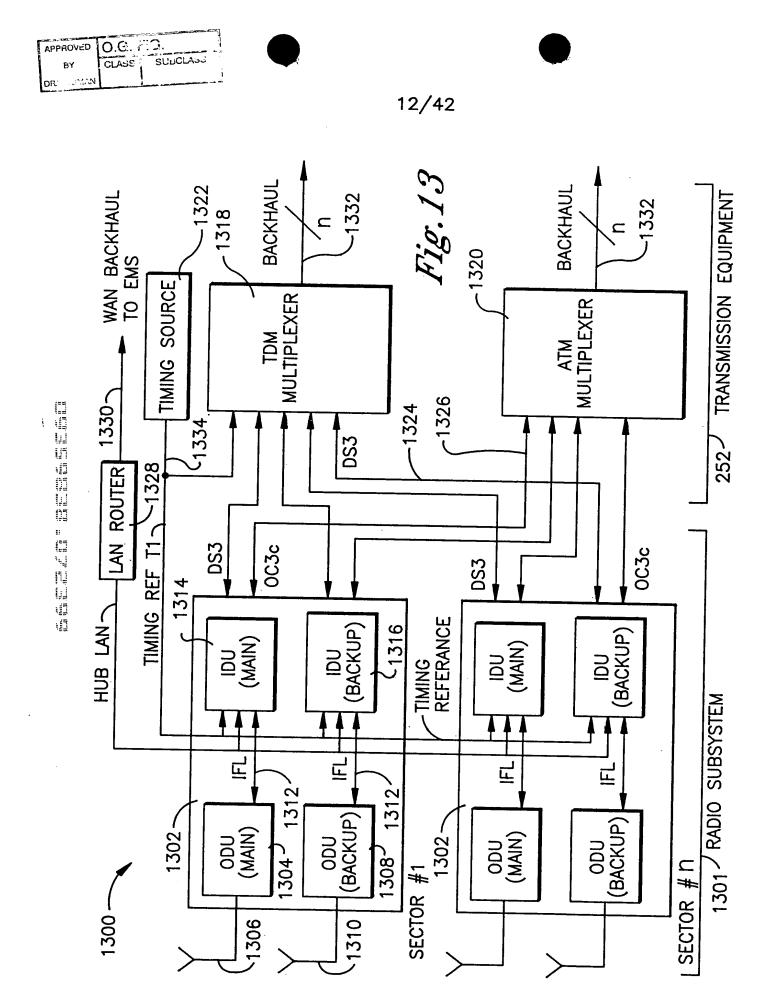




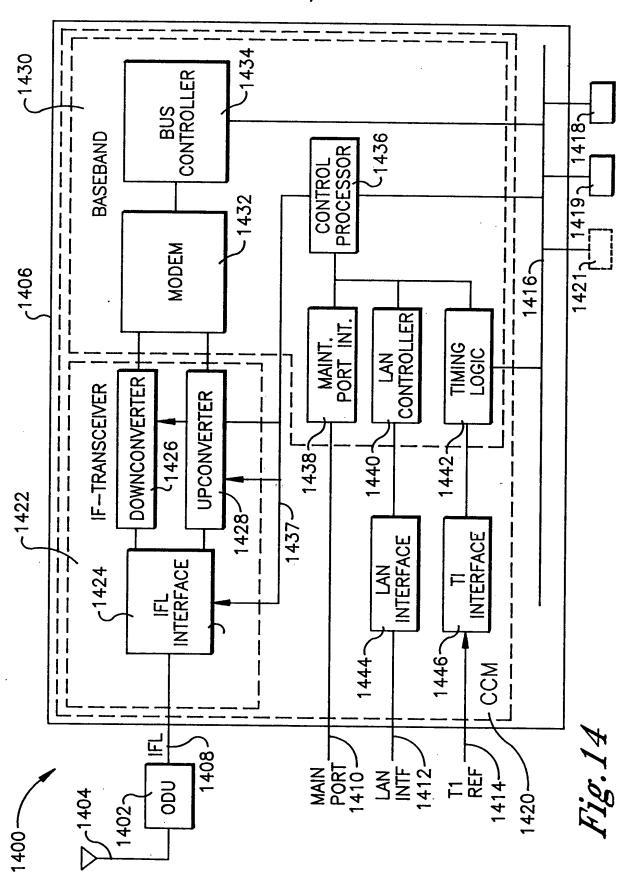




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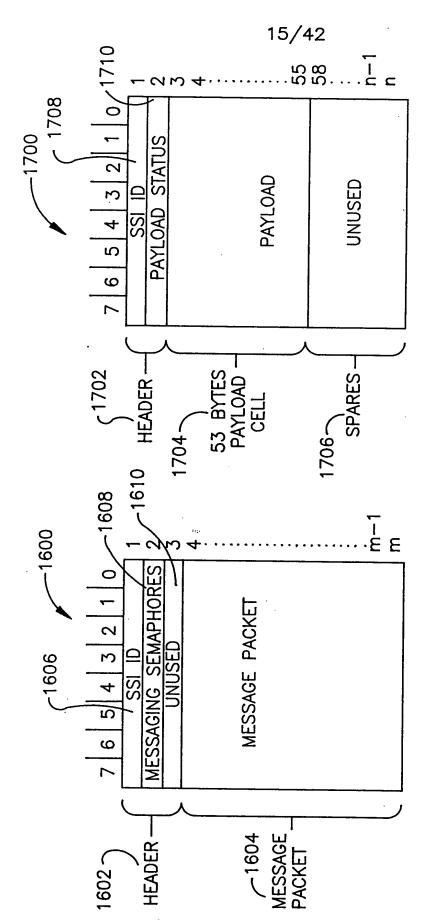
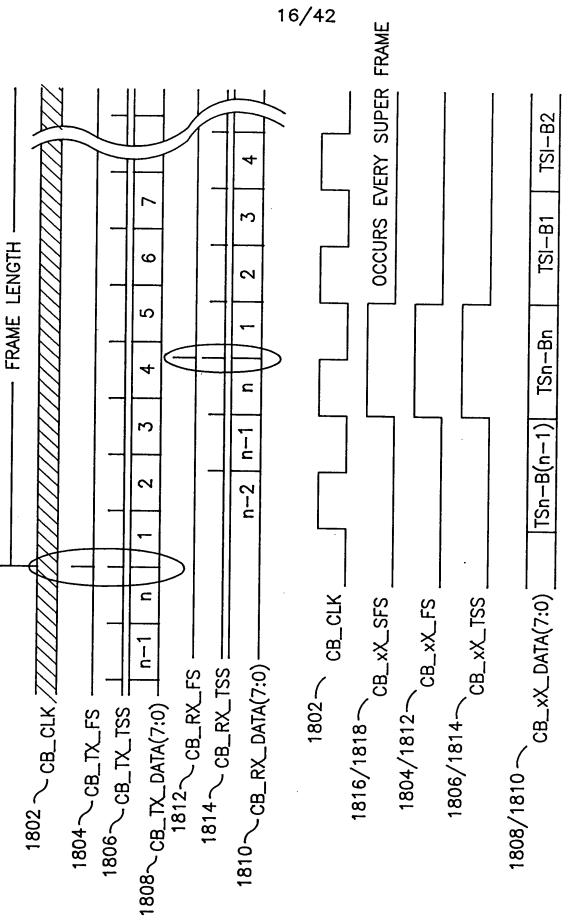


Fig.

Fig. 16



CELL BUS TIMING

Fig. 18

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Ŋ 4 M 1-1 2 n-2 TSI-B4  $\Box$ n-1 TSI-B3 n-2

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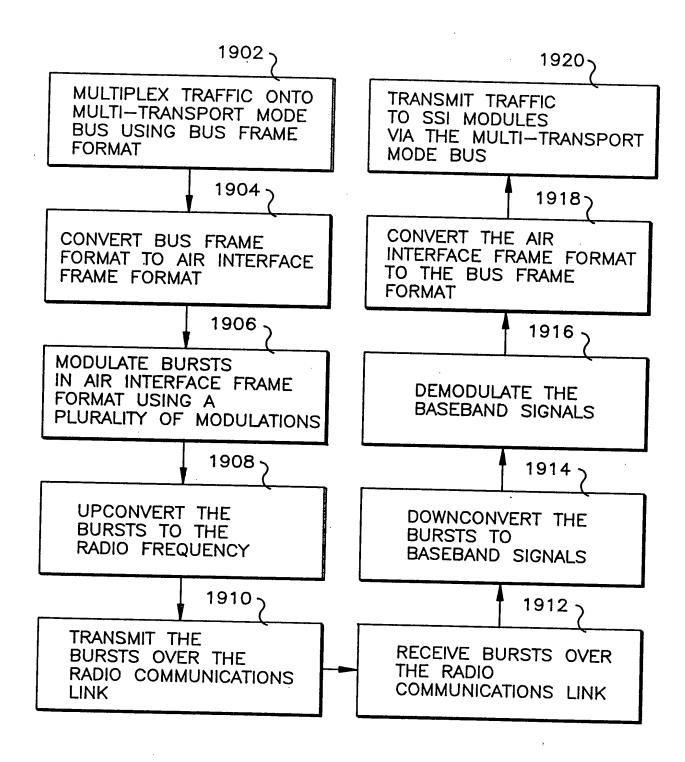
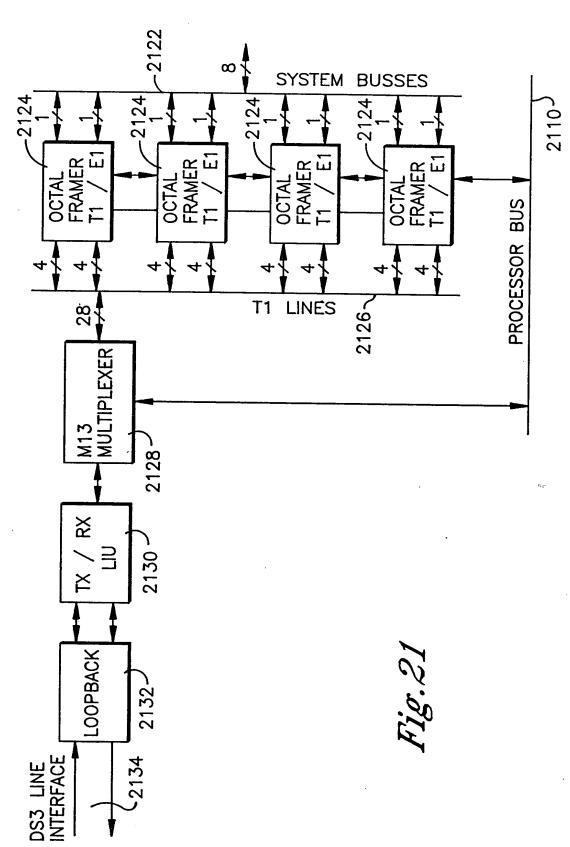


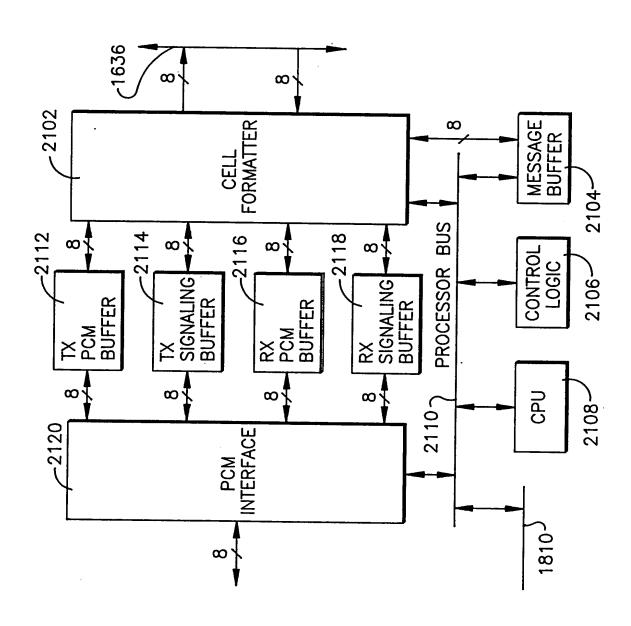
Fig. 19

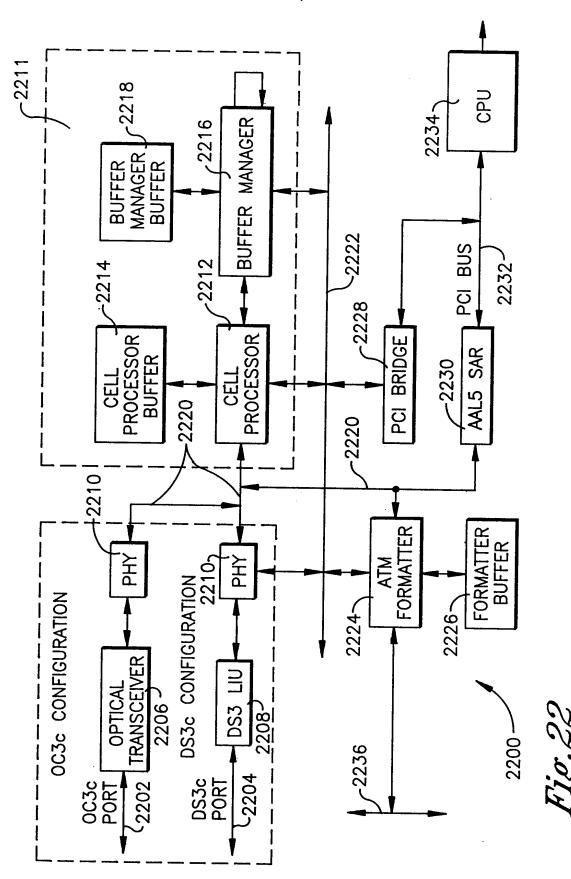
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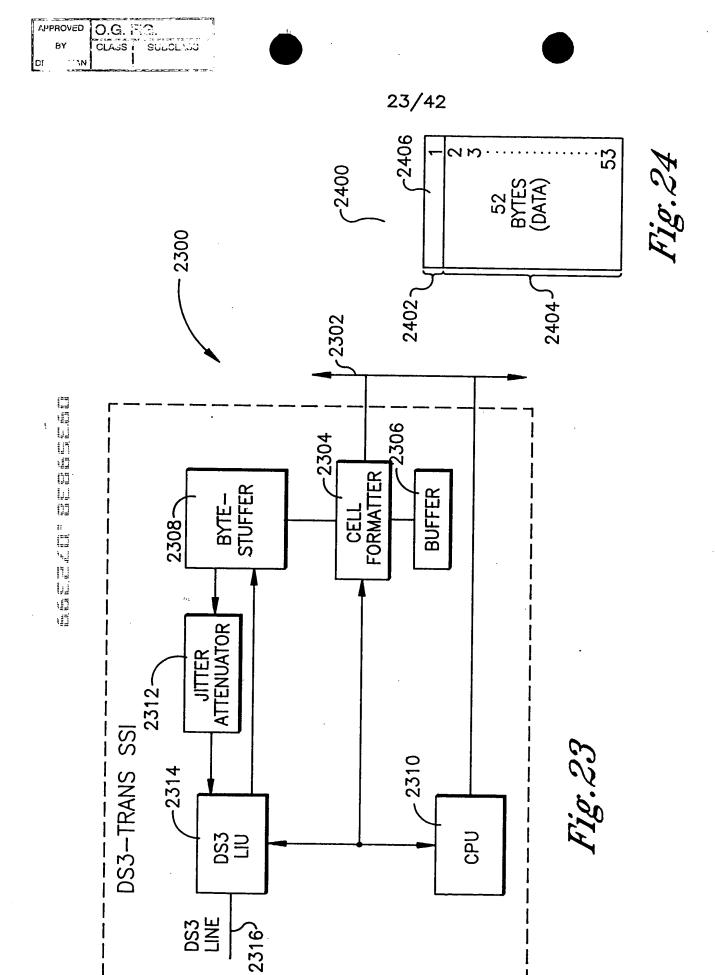


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BY	CLASS	SUBCLAS3
DR 3MAN		

Fig.21







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T1/E1 LINE INTERFACE

AND FRAMER

-2554

INTERFACE

FRAMER

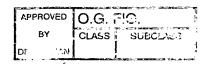
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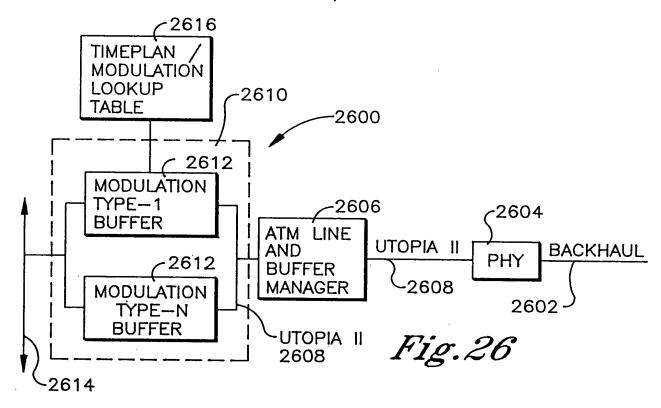


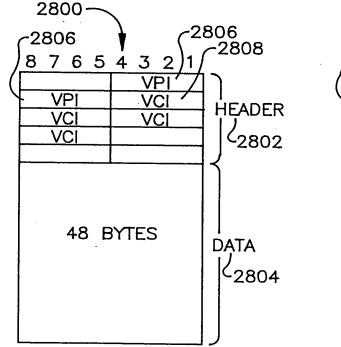
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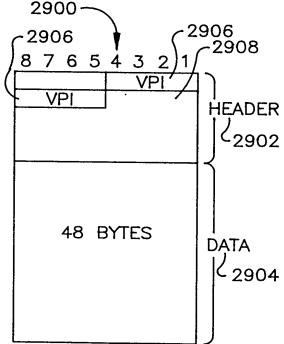




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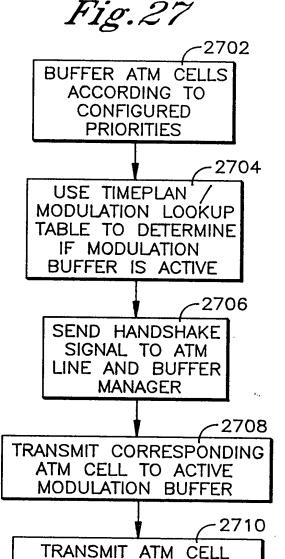






ATM CELL Fig. 28

Fig.29



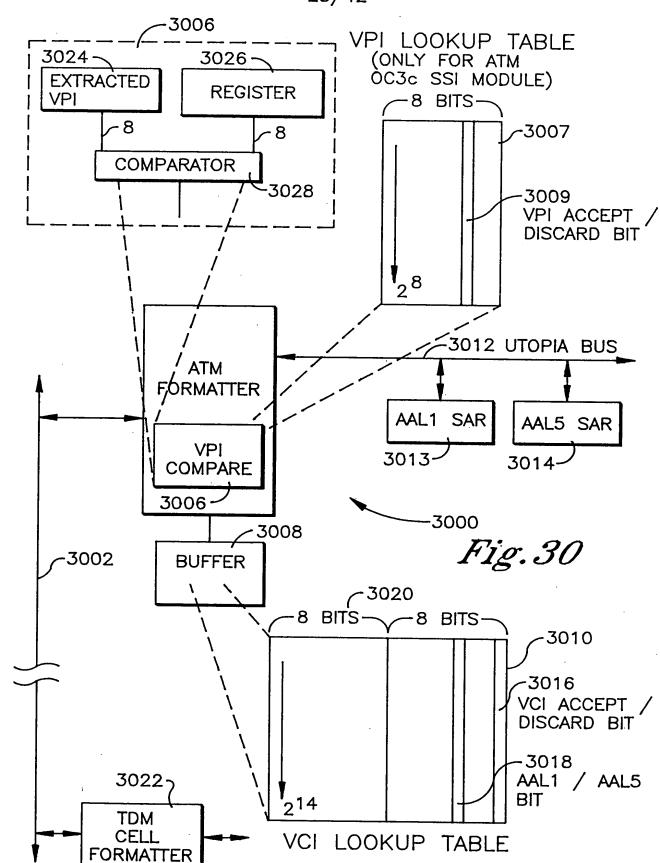
ONTO MULTI-TRANSPORT MODE CELL BUS OF RADIO SYSTEM

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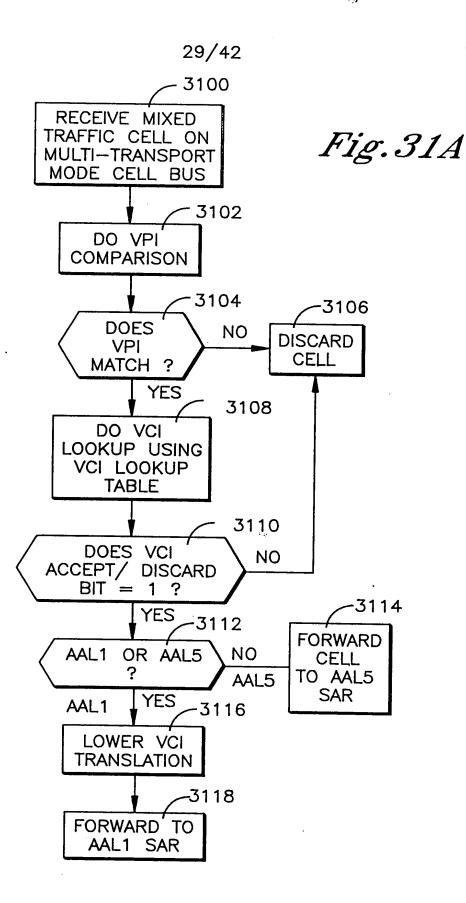
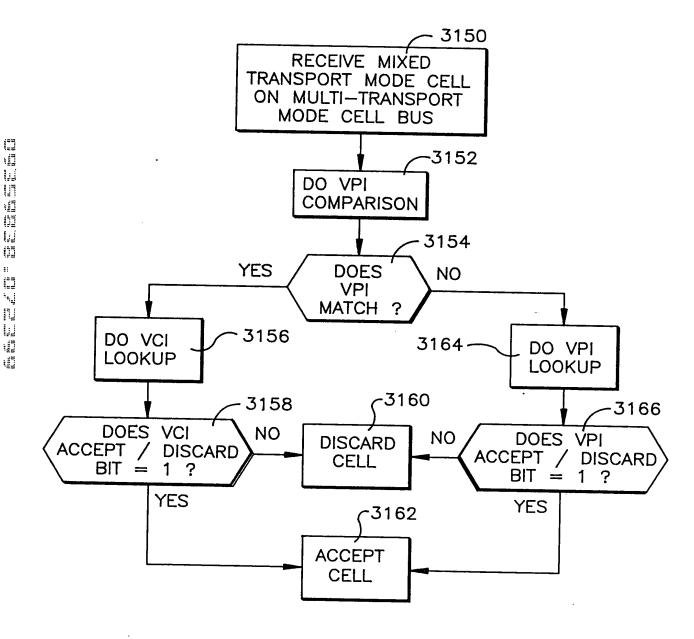
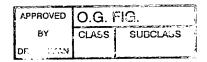


Fig. 31B



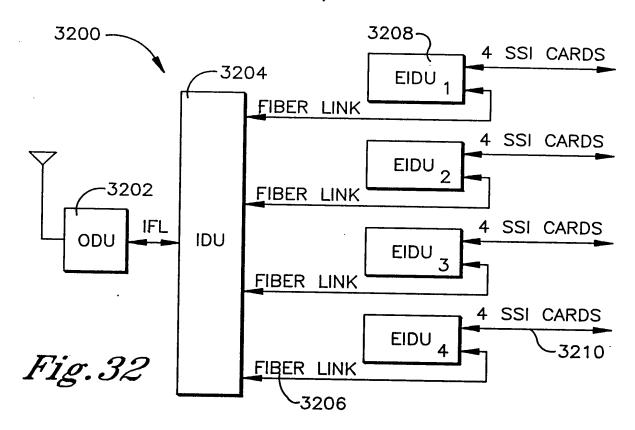
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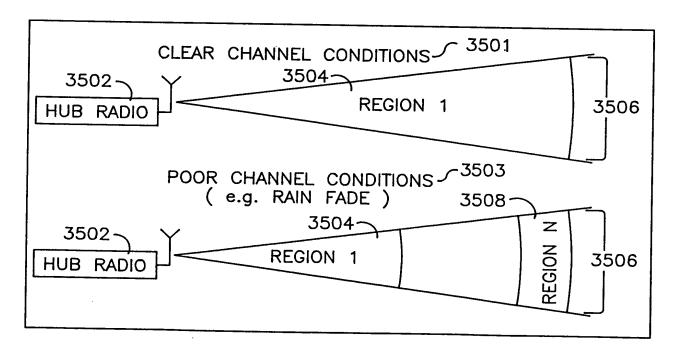
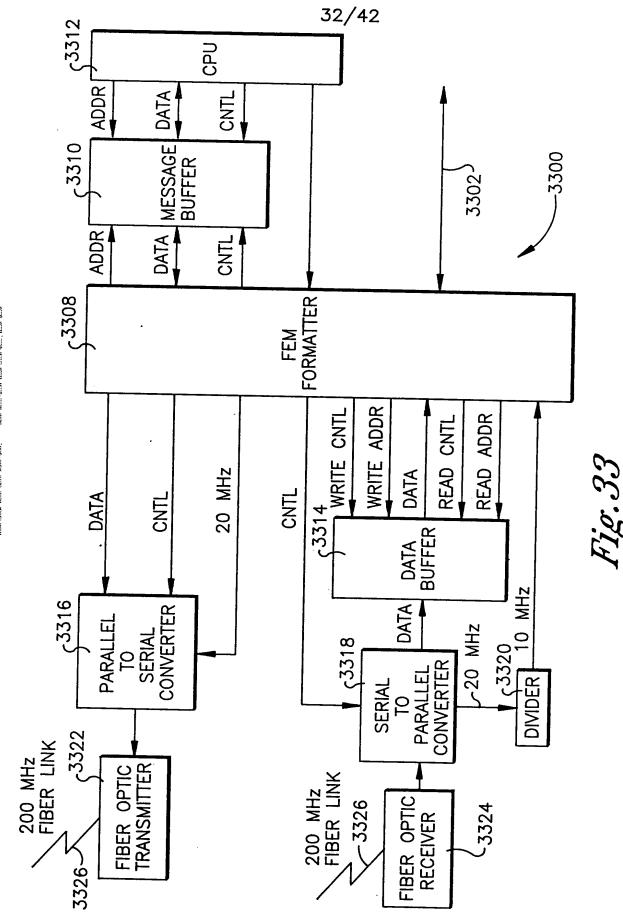


Fig. 35



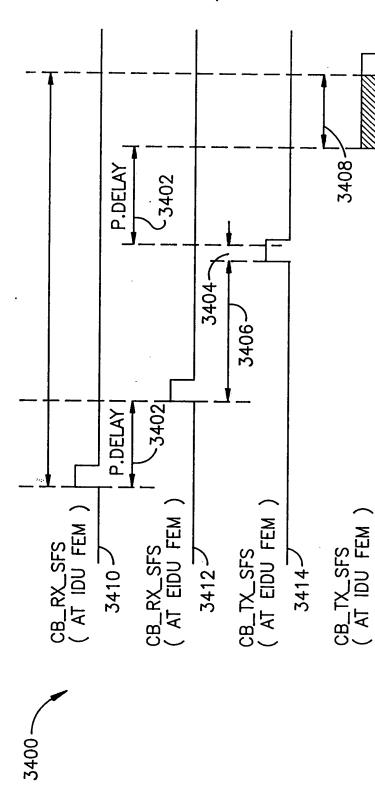
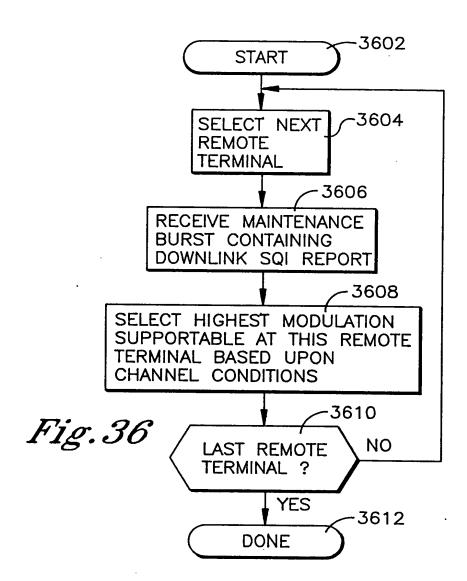
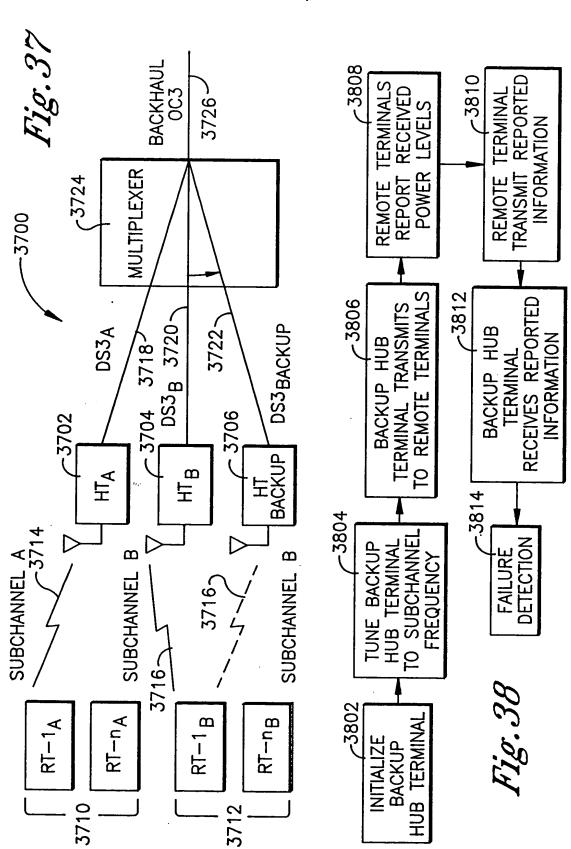


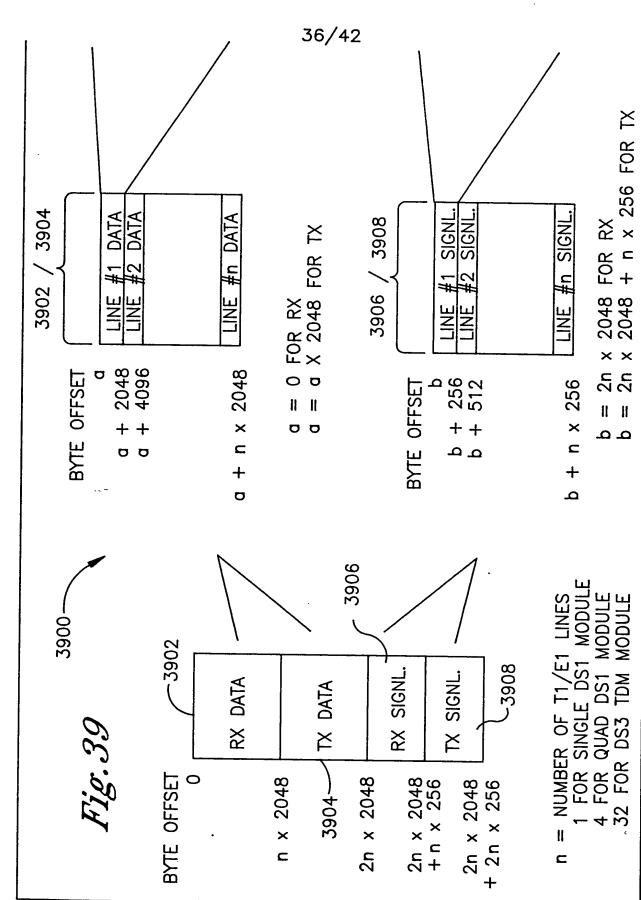
Fig. 34

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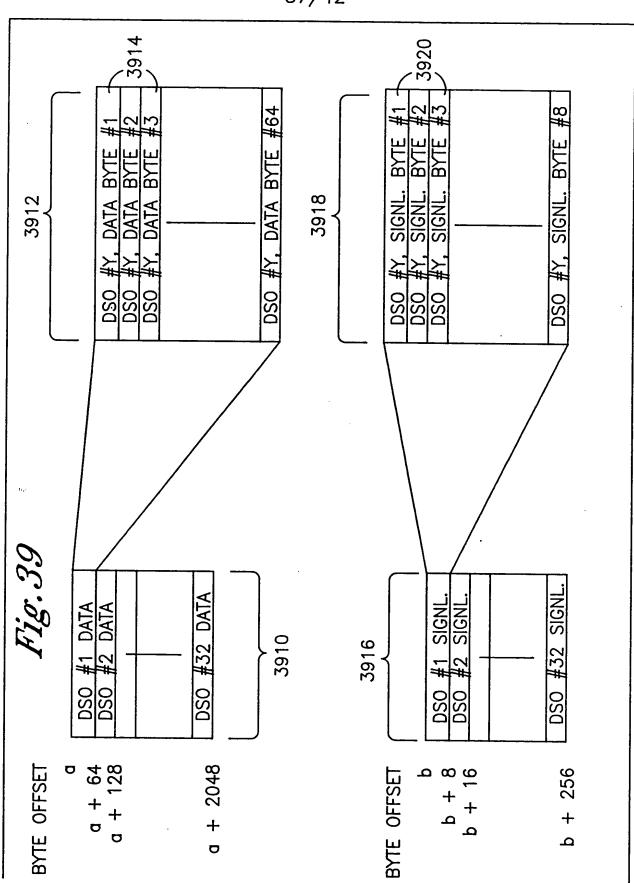


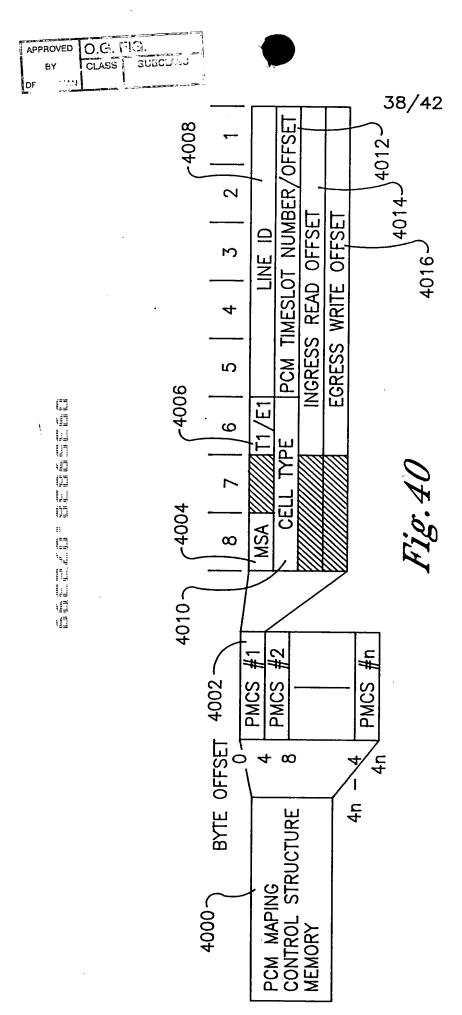
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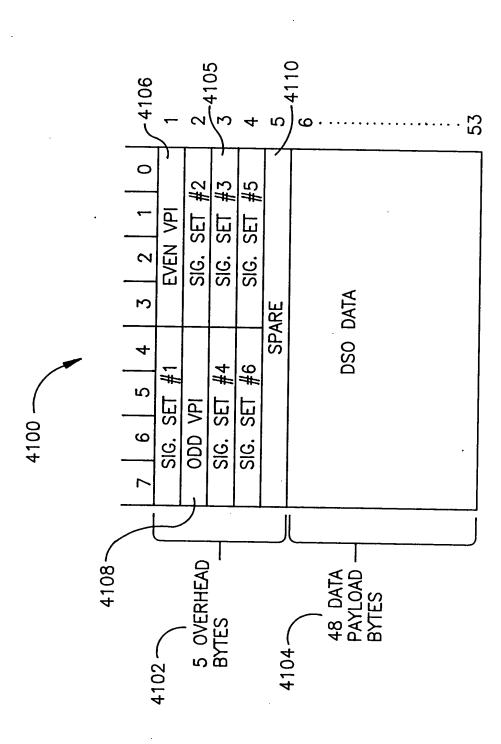
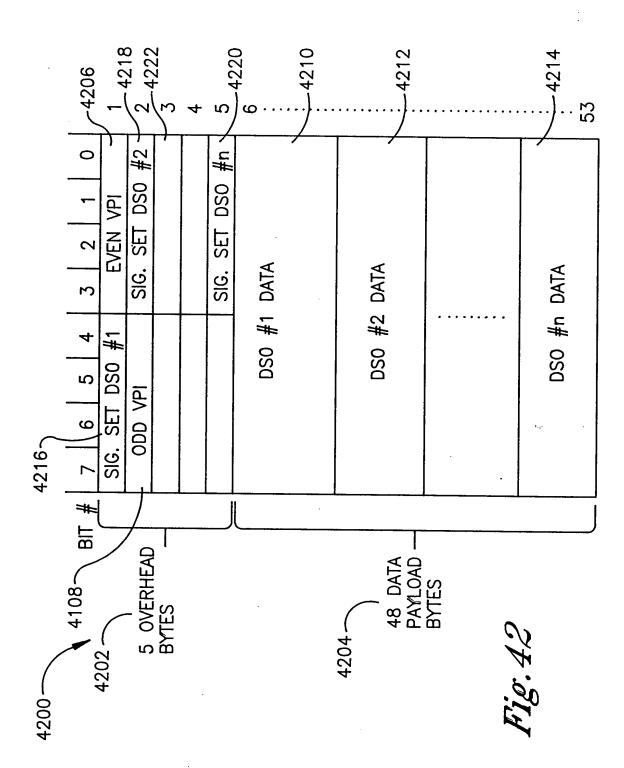


Fig. 41

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52 50 51 വ 9 0 G.802 FRAMING BYTE #2 EVEN VPI SPARE DSO #24, FRAME #2 G.802 FRAMING BYTE DSO #24, FRAME #1 #2 DSO #1, FRAME #2 DSO #1, FRAME #1 ~ #2, FRAME #2, FRAME 3 SPARE 4310 DS0 DS0 Ŋ ODD VPI SPARE ဖ 1 3 OVERHEAD BYTES <sup>-</sup> 50 DATA PAYLOAD -BYTES 4308 4300 -

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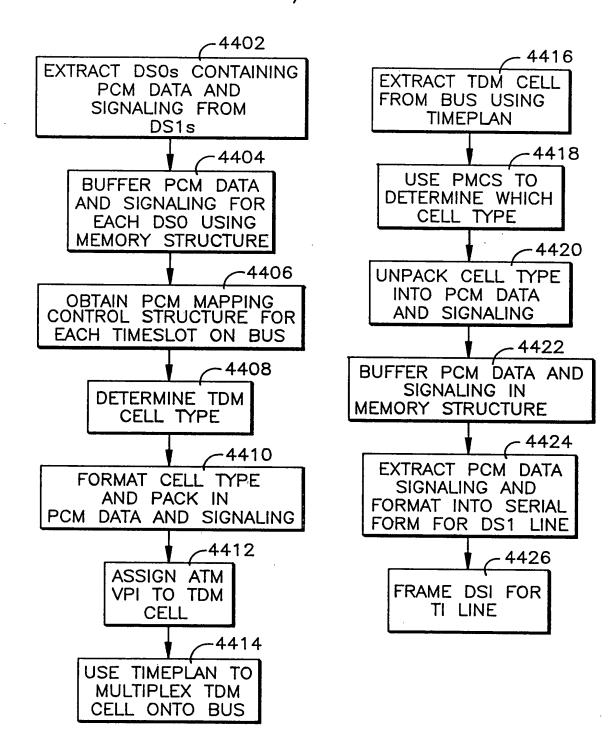


Fig. 44A

Fig. 44B